REMARKS

This is intended as a full and complete response to the Office Action dated August 25, 2003, having a shortened statutory period for response set to expire on November 25, 2003 (the "Office Action"). Claims 7-9 have been canceled without prejudice. Claims 1-6 remain in the application, and new claims 10-14 have been added.

In the Office Action, claims 1-2, 4-7, and 9 were rejected under 35 USC 102(b) as being anticipated by Akao (U.S. Pat. No. 5,307,464; "Akao"). With respect to claims 7 and 9, those claims have been canceled without prejudice, and thus this rejection is moot with respect to those canceled claims.

Akao discloses a selection of information for defining a peripheral function and writing a program into non-volatile memory elements in a sub-processor (*see*, Akao at Figure 8 or Figure 9). Figure 1 of Akao shows non-volatile memory elements, such as ROM 4, and shows sub-processor 5. Figure 2 of Akao is a lower-level diagram of sub-processor 5. In Akao, a peripheral function is "…retrieved from storage media…" and written into "non-volatile memory elements 13 and 62 of the sub-processor 5 embedded in microprocessor 1…" (*id.*).

Amended Claim 1 has among other features, a processor core and a configurable logic block coupled to the processor core. Assuming arguendo, as the Office Action asserts, that Akao discloses a sub-processor that is a configurable peripheral device, nothing in Akao teaches or suggests a configurable logic block coupled to the processor core. Thus claim 1 should be allowable.

Accordingly, it is respectfully submitted that amended claim 1 is not shown or described by Akao, and is thus allowable in view of Akao. Additionally, claims 2-5,and 14 which depend upon amended claim 1 should be allowable for at least the same reasons claim 1 is allowable.

With respect to claim 4 as originally presented, the Office Action states in relevant part that "…Akao discloses the peripheral and bus are implemented on a FPGA (see Figs. 15-17

and 20)." Figure 15 of Akao is for a ROM (col. 16, line 40-41). Figure 16 is for a memory (col. 17, lines 45-47). Figure 17 of Akao is for a RAM (col. 19, lines 53-60). Figure 20 of Akao is a sub-circuit for selecting a next address register of Akao's sub-processor. None of these listed figures, nor any of the figures in Akao, show or suggest an FPGA. Accordingly, it is respectfully submitted that the rejection of original claim 4 in view of Akao is without support with respect to the Figures of Akao relied upon in the Office Action and should be withdrawn.

Claim 6 recites in part the programmable logic device comprising a processor core. Nothing in Akao discloses or suggests such a feature. Accordingly, it is respectfully submitted that amended claim 6 is thus allowable in view of Akao. Additionally, claims 10-13, which depend upon amended claim 6, should be allowable for at least the same reasons claim 6 is allowable.

In the Office Action, claims 1, 4, and 6 were rejected under 35 USC 102(b) as being anticipated by Basset (U.S. Pat. No. 5,812,867; "Basset"). In Basset, one or more peripheral circuits include "option circuits" for "enabling the operation" of such one or more peripheral circuits (*see*, Basset at the Abstract). Peripheral circuits are put into service by linking them to programmable memory (*id.*). Basset neither discloses a configurable logic block, hence claim 1 should be allowable.

Accordingly, it is respectfully submitted that amended claim 1 is not shown or described by Basset, and is thus allowable in view of Basset. Additionally, claims 2-5, which depend upon amended claim 1 should be allowable for at least the same reasons claim 1 is allowable.

More particularly, with respect to claim 4 as originally presented, the Office Action states in relevant part that "...Basset discloses the configurable peripheral device and bus are implemented on a FPGA (see Fig. 7)." Figure 7 of Basset shows an option circuit 6 connected to a bus 15, which is coupled to a microprocessor 1 through pass gate transistors 49. Option circuit 6 includes two registers 43 each of which is

coupled to a respective trace of bus 15 via inverters 44 and 45 "mounted back-to-back" (*e.g.*, cross-coupled inverters) and pass gate transistors 46. Accordingly, an FPGA is not shown in Figure 7 of Basset, or any other figure in Basset. Furthermore, Basset does not suggest an FPGA or any other known type of programmable logic device. Accordingly, it is respectfully submitted that the rejection of original claim 4 in view of Basset is without support and should be withdrawn.

Claim 6 recites in part the programmable logic device comprising a processor core. As indicated for claim 4 above, nothing in Basset discloses or suggests such a feature. Accordingly, it is respectfully submitted that amended claim 6 is thus allowable in view of Basset. Additionally, claims 10-13, which depend upon amended claim 6, should be allowable for at least the same reasons claim 6 is allowable.

In the Office Action, claims 2-3, 5, and 7-9 were rejected under 35 USC 103(a) as being obvious over Basset in view of Mattheis *et al.* (U.S. Pat. No. 6,085,337; "Mattheis"), Davidson *et al.* (U.S. Pat. No. 5,428,748; "Davidson") or "applicant's admission (page 4, ll. 4-10)." The reasons for allowance of amended claim 1 as set forth above are incorporated here by reference with respect to this rejection. Accordingly, as amended claim 1 is allowable over the primary reference of Basset, likewise claims 2-3 and 5 are allowable over the reference of Basset in combination with any of Mattheis, Davidson or Applicant's prior art labeled Figure 2A. With respect to claims 7-9, those claims have been canceled without prejudice, and thus this rejection for obviousness is moot with respect to those canceled claims.

Accordingly, it is respectfully submitted that the references cited by the Examiner, neither alone nor in combination, teach, show, or suggest the claimed invention. Having addressed all issues set out in the Office Action, Applicant respectfully submits that the claims are in condition for allowance and respectfully request that the claims be allowed.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on November 24, 2003.

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